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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/753,103	CHEN ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 2/26/07 and Replacement Sheet for Figure 1 filed 12/07/06 form the basis for this office action. In said Amendment Applicant substantially amended claims 3, 9, 10, 11, 17 and 21 and amended the Specification. Comments on Remarks are found below under "Response to Arguments".

Specification

1. The abstract of the disclosure is objected to because the abstract ends with the word "and" and fails to have a period at the end. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claims 1-13 and 15-22 and 24*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (6,911,690 B2) (as previously made of record by examiner, see PTO-892) in view of either Prior Art as Admitted by Applicant and Chapman et al (6,118,161), and, - in an alternative rejection, over Sakui et al (6,411,548 B1) and Chapman et al (6,118,161).

Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source region 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source region, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source region (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a bitline, inherently is contacted with a bitline, "bitline diffusion" being a diffusion region for contacting the bitline, thus requiring a bitline contact: both bitline and bitline contact must therefore exist; that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8) (N.B.: Matas et al is cited here for establishment of fact, not for teaching).

Hsu et al do not necessarily teach the last select gate in the row at least partially overlaps said source region. *However, it would have been obvious to include said*

limitation in view of either Prior Art as Admitted by Applicant (Figure 1 in the specification, see "Background of the Invention") or Sakui et al (Figure 47, and col. 27, lines 43-49), who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region overlap (Figure 1 and legend (page 4) and pages 1-3 of the specification by applicants, and in the alternative: Figure 49 and column 27, lines 43-49 in Sakui et al) (with regard to Sakui et al: otherwise no overlap capacitance could exist). *Motivation* to include said teaching of overlap, between any select gate and source region derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any other MOS transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 2: clearly stacked gates and select gates are aligned to each other. The term "self-aligned" refers to the process of self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 3: The memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates and control gates.

Hsu et al do not necessarily teach said tunnel oxide being thinner than the first and second dielectrics. However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling, i.e., the explicit teaching of "tunnel oxide" means that the oxide layer is so thin that quantum-mechanically the layer can be crossed or penetrated although the charge carrier's energy is lower than the barrier energy (see, e.g., Bohm, "Quantum Theory", 1951, ISBN: 0-486-65969-0; pages 238-240, cited for establishment of fact, not for teaching). Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 4: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a

short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages. .

On claim 5: Referring to the rejection under 35 U.S.C. 112, second paragraph, the claim is interpreted without giving weight to the limitation "high". Inherently, erase paths based on Fowler-Nordheim tunneling as exploited by Hsu et al extend from the floating gates, through the tunnel oxide to the channel regions by virtue of the very existence of a current path for electrons between floating gate to the channel regions through Fowler-Nordheim tunneling (col. 8, l. 61-67), and voltage is coupled to the floating gates both from the control gates and from the select gates (keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin).

On claim 6: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because regions are conductive through the action of said gates, thereby allowing programming paths to exist); and voltage is coupled to the floating gates both from the control gates and from the select gates on the sides of the stacked gates toward the source region (col. 3, l. 50-56): keep in mind the tunnel oxide does not reduce the voltage in the floating gate by any meaningful way from the voltage in the channel because it is extremely thin. It is noted that the newly added limitations "below the floating gates" and "in the substrate" are met in any channel with lateral floating gates: the channel is located in the uppermost portion of the substrate abutting the interface between substrate and gate

insulating layer. Therefore, said newly added limitations do nothing to further limit the cell array.

On claim 7: Program paths extend from off-gate channel regions between the select gates and the floating gates to the floating gates (because channel regions are highly conductive through the action of the gates and hence substantially conductive, thereby allowing programming paths to exist), while the remainder of the limitation defined by claim 7 constitutes functional language: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 8: The select gates in unselected cells *can be* biased at a relatively high voltage to turn on the channels beneath them to form a conduction path between the bit line diffusion and the source diffusion. Whether or not they are has no patentable weight: In reference to the claim language referring to said limitation, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re

Otto , 136 USPQ 458, 459 (CCPA 1963). In the underlying case no difficulty exists in the prior art structure to impart the voltages as claimed because the select gates are independent of each other.

On claim 9: The bit line for a row containing a selected cell to be programmed *can be* held at 0 volts because said bit line is conductive; a relatively low positive voltage *can be* applied to a cell select gate for the selected cell as the select gates are independent; a relatively high positive voltage *can be* applied to the source diffusion at the second end of the row in which the selected cell is located because any source region is inherently conductive; a relatively high positive voltage *can be* applied to the control gate in the selected cell; a relatively high positive voltage *can be* applied to the select gates for unselected cells, and a relatively high positive voltage *can be* applied to the control gates in the unselected cells. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 10: An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the bit line diffusions, the source diffusion and the P-well at 0 volts. Whether this is done has no patentable weight. In reference to the claim language referring to application of

voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 11: An erase path *can be* formed by a relatively high negative voltage on the control gates and a relatively low negative voltage on the select gates, with the active area at a positive voltage and the bit line and source diffusions floating. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 12: A read path *can be* formed by turning on the select transistors and the stacked control and floating gate transistors in unselected cells (cell selection being possible in the structure defined by Figures 3 and 4a,b), with the common source at 0 volts, the bit line diffusion at 1-3 volts, and the control gate at relatively high positive voltage, and the control gate of the selected cell *can be* biased at 0-1.5 volts to form a conduction channel under the floating gate for an erase state and a non-conduction channel for a program state: application of a voltage on the control gate does improve

the conductivity of the channel while for any non-vanishing conductivity in the channel and any non-zero voltage on the bitline diffusion relative to the source region a positive amount of current is known to flow between bitline and source: inherently so, because electrons in the channel respond to the positive gate voltage by forming a thin layer of enhanced conductivity along the connection between source and drain (bitline diffusion), i.e., a conduction channel under the floating gate. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 13: As discussed under claim 11, an erase path *can be* formed by biasing of control gates and select gates; since this biasing can be done for each individual member in the cell array an erase path can erase the whole cell array simultaneously; and since cells can be selected individually a program path which is single cell selectable *can be* created through appropriate biasing. Whether this is done has no patentable weight. In reference to the claim language referring to application of voltage as recited in the claim language, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the

prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

On claim 15: Hsu et al teach a NAND flash memory cell array (Figures 1A, 1B, title, abstract and column 4, line 55 – column 6, line 24), comprising:

a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) positioned above a floating gate 118 (column 5, line 36). Furthermore, a bitline diffusion, i.e., diffusion region for a bitline, inherently is contacted with a bitline: both bitline and bitline contact, if only in the form of a contact interface, must therefore exist; that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8).

Hsu et al do not necessarily teach the last select gate in the row being directly above said source region. *However, it would have been obvious to include said limitation in view of Sakui et al,* who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region showing said select gate directly above said source diffusion (i.e., a vertical line may be drawn intersecting both source diffusion and select gate (Figure 49; see also column 27, lines 43-49) (otherwise no overlap capacitance could exist). *Motivation* to include said teaching derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by Chapman et al (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 16: clearly stacked gates 118/122 and select gates 106 are aligned to each other (see Figures 1A and 1B). The term "self-aligned" refers to the process of "self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 17: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates and control gates. *Hsu et al do not necessarily teach* said (necessarily and inherently extremely thin) tunnel oxide being thinner than the first and second dielectrics.

However, the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 18: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates; , in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages.

On claim 19: Hsu et al teach a NAND flash memory cell array, comprising: a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), bit line diffusions 124 (col. 5, l. 63) and source diffusions 126 (col. 5, l. 65) spaced alternately ("alternately" here interpreted as "arranged one alongside the other") in the active area

with no other diffusions between them, a plurality of stacked gates 118/120 (col. 5, l. 3-5) and select gates 106 (col. 5, l. 27) arranged alternately ("alternately" here interpreted as "arranged one alongside the other") in rows between the bitline diffusions and the source diffusions (Figure 1A), with each of the stacked gates having a control gate 120 (col. 5, l. 27) positioned above a floating gate 118 (col. 5, l. 36). Furthermore, any bit line diffusion is inherently in contact with a bit contact and bit line contacts interconnecting the bit lines and bit line diffusions (diffusion being a region in the substrate wherein impurities have been diffused to establish a region of elevated electrical conductivity so as to serve as electrical contact to the bit line), as seen, for instance from the description and definition of the prior art through Figure 1 in the Specification (see pages 1-3 and Figure 1 in the Specification); that the limitation "a bitline above the row, and a bit line contact interconnecting the bit line and the bit line diffusion" is inherent is also witnessed by Matas et al ("Memory 1997", by Integrated Circuit Engineering Corp., ISBN: 1-877750-59-X), Section 10, "Flash Memory Technology", pages 10-1 through 10-16, see especially page 10-5 on the NAND cell in Flash Memory chips, this review of the various memory devices including NAND flash memory chips showing a bitline bending down into a bitline contact contacting a bitline diffusion to the left of the leftmost select gate (Fig. 10-8).

Hsu et al do not necessarily teach "the last select gates in each of the rows at least partially overlapping the source diffusions between the rows".

However, it would have been obvious to include said limitation in view of either Prior Art as Admitted by Applicant (Figure 1 in the specification, see "Background of the

Invention") or Sakui et al (Figure 47, and col. 27, lines 43-49), who, in a patent on a NAND flash memory device, - hence analogous art, teach NAND flash memory device with select gate – source region overlap (Figure 1 and legend (page 4) and pages 1-3 of the specification by applicants, and in the alternative: Figure 49 and column 27, lines 43-49 in Sakui et al) (with regard to Sakui et al: otherwise no overlap capacitance could exist). *Motivation* to include said teaching of overlap, between any select gate and source region derives from the well-known circumstance that for low resistance and good performance the gate should slightly overlap with the source, as witnessed by the teaching of *Chapman et al* (column 4, lines 21-28). In this regard it is noted that the select gate in any NAND flash memory device is no different from an ordinary gate in any transistor in that its role is to regulate the channel conductivity so as to select the channel to be open or closed.

On claim 20: clearly stacked gates and select gates are aligned to each other. The term "self-aligned" refers to the process of self-alignment", which is a process limitation and does not further distinguish the array as device as claimed by Applicant, but instead only further limits its process of making.

On claim 21: the memory cell array by Hsu et al includes a relatively thin tunnel oxide 116 (column 5, lines 46-57) between the floating gates and the substrate (abstract), a first dielectric 114 (column 5, lines 3-25) between the floating gates and the select gates, and a second dielectric 122 (column 5, lines 6-57) between floating gates and control gates. *Hsu et al do not necessarily teach* said (necessarily and inherently extremely thin) tunnel oxide to be thinner than said first and second dielectric. However,

the function of said tunnel oxide requires said tunnel oxide to be extremely thin so as to have a spatial scale in the thickness direction that is in the quantum regime so as to allow tunneling. (see, e.g., Bohm, "Quantum Theory", 1951, ISBN: 0-486-65969-0; pages 238-240, cited for establishment of fact, not for teaching). Therefore, great care has to be taken to make said tunnel oxide extremely thin. No such functional requirement is needed for either said first dielectric 114, which is a spacer and hence only functions to provide sizable space between other objects, nor for said second dielectric 122, which serves to separate the control and floating gates, of course also on a non-quantum-mechanical but instead classical scale. In conclusion, both for functional and for cost considerations it does not make sense to select the thickness of either first or second dielectric layers 114 and 122, respectively, to be of quantum-mechanical size and hence it is obvious to make said first and second dielectrics thick relative to the tunnel oxide.

On claim 22: Any value of intergate capacitance different from zero (excluded here because the gates are (a) conductive and (b) flank an insulation layer sandwiched between said gates) implies a voltage coupling between the gates, in particular inter-gate capacitances between select gates and floating gates and between control gates and floating gates (see Figure 1B, showing said select and floating gates to be only a short distance apart, while having independent voltages, and showing said control gate and floating gates to be only a short distance apart, and having independent voltages.

On claim 24: *Hsu et al teach*:

a NAND flash memory cell array, comprising: a substrate 100 (column 4, line 66) having an active area 104 (column 4, line 67), a bit line diffusion 124 (column 5, line 63) and a source diffusion 126 (column 5, line 65) in the active area with no other diffusion in the active area between the bit line diffusion and the source diffusion, a plurality of stacked gates 118/120 (column 5, lines 3-5 and 36-45) and select gates 106 (column 5, lines 1-4) arranged alternately in a row above the active area between bitline diffusion and source diffusion (Figure 1B), with each of the stacked gates having a control gate 120 (column 5, line 27) and a floating gate 118 (column 5, line 36) with aligned sides adjacent to the select gates (Figure 1B), erase paths between the floating gates and channel regions in the active area beneath the stacked gates (col. 8, lines 61-67).

The limitation "self-aligned" rather than merely "aligned" only further introduces a limitation on the method of making said memory cell array and fails to further limit the invention claimed here as a final structure only. The distinction between "aligned" and "self-aligned" thus constitutes a product-by-process limitation and is non-limiting. A product by process limitation is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Furthermore, voltage coupling from the control gates to the floating gates inherently exists because the control gates control by definition the voltage of the floating gates so as to control the number of charge carriers in said floating gates while voltage coupling between select gates and floating gates inherently exists because the select gates determine whether or not a channel exists along which charge carriers can approach said floating gates.

Response to Arguments

Applicant's arguments filed 2/26/07 have been fully considered but they are not persuasive.

The Objection to the Drawing has been withdrawn in light of Replacement Sheet filed 12/07/06.

Although Applicant alleges the Abstract has been amended to overcome the objection to the Specification (section 1 of the previous action on the merits) examiner cannot find any amendment to the Abstract in said Amendment. The objection to the Specification on the abstract therefore stands. Examiner contacted Electronic File staff, but said staff only was able to confirm that no such amendment to the Abstract is available.

The rejections of claims 3, 17 and 21 under 35 USC 112, 2nd paragraph, have been overcome by amendment.

The rejections of claims 4, 18 and 22 have been withdrawn because, in the absence of any quantification, any inter-gate capacitance is large enough for some

voltage coupling between the gates during program and erase operations. Examiner realizes there is no possibility, in light of the Specification, to provide the necessary quantification to provide meaning to the cited limitation.

The rejections under 35 USC 112, 2nd paragraph, of claims 3, 9, 10, 11, 17 and 21 have been overcome by amendment.

With regard to the rejections under 35 USC 103(a), Applicant argues that "Examiner continues to misconstrue and mischaracterize what is actually found in the references, and he continues to try to combine selected elements from the different references (and now from Applicant's own disclosure) when there is no basis for doing so", and specifically that in Hsu et al there "are no bit lines, bit line diffusions or bit line contacts", appears to have missed the essence of the Response to Arguments ad 3), page 25 of the previous office action, where examiner provided evidence through Matas et al that said bit lines, bit line diffusion and bitline contact are inherent in the NAND Flash Memory cell array (col. 4, l. 61) of Hsu et al, while Hsu et al itself is quoted for the bit line diffusion (element 124) and Matas et al through page 10-5 specifically point out that the bit line is above the row and is seen to contact the bit line diffusion. There appears no reason at all to wonder, as applicant does, why element 124 is a "bit line diffusion", this being a matter of words only. See Hsu et al, col. 8, l. 55 for evidence that the "drain" is part of a "bit line". That Hsu et al do not teach overlap is acknowledged in the rejection and hence requires no further commentary.

Counter to applicant's argument that "nowhere in the prior art is there any suggestion of bit line and source diffusions at opposite ends of a row of alternating

stacked gates and select gates with no other diffusions in the active area between the bitline diffusion and the source region", between bitline diffusion 124 and source region 126 there are no other diffusion regions ("diffusions" in applicant words) in Hsu et al, while said alternating stacked gates and select gates are immediately evident in Hsu et al (see the cited 118/120 for stacked gates and 110 for select gates). Applicant asks: "Even if such elements (sic) were inherent in the device by Hsu et al, where would they be?" Interpreting "such elements" in the widest possible manner, this is where they are in the NAND Flash Memory Device by Hsu et al: bitline diffusion: 124, bitline contact inherently contacting said bitline diffusion by making contact to the upper main surface of said bitline diffusion (see Matas et al, page 10-5, Figure 10-8): downward bent portion of bitline (Aluminum)), and bitline: "Bitline (Aluminum) in Matas et al, straight portion overlying the plurality of alternating stacked gates 118/120 and select gates 110. No motivation is necessary because the only parts missing in Hsu et al in this regard are inherent in a NAND Flash Memory cell array as witnessed by Matas et al. As to applicant's question "how would the device work", NAND Flash Memory cell arrays would NOT work in the absence of providing a bit line contact contacting the drain diffusion region alias bitline diffusion) to a bit line array. Applicant appears to treat the rejection as if the elements shown by Hsu et al and those that are inherent in it according to Matas et al require some statement on motivation and combinability, in apparent misinterpretation of the role of Matas et al to show inherency of the bit line contact and bit line given the drain (= bit line diffusion) region in the NAND Flash Memory cell array by Hsu et al.

On applicant's comment on Sakurai, Sakurai et al need not suggest the limitation missing in Hsu et al AND in a device having the other elements. Motivation derives from the teaching by Chapman et al, which is known by those of ordinary skills in the art. Here, as everywhere else in applicant's discussion, it appears that a person of ordinary skill in he art merely would know how to spell words, and that when words selected by applicant are not spelled out then the limitation is not met. This is a gross underestimate what is meant by "one of ordinary skill in the art", as also recently pointed out by the Supreme Court decision No. 04-1350 KSR International Co. v. Teleflex Inc et al; from which decision it is clear even more so than before that when a person of ordinary skill in the art could have combined Hsu et al with at least partial overlap of gate and select gate as disclosed by Sakui et al (see reference to col. 27, l. 43-49 in the previous office action) and would have seen the benefits of doing so (i.e., achieving low resistance and good performance as known in the art of insulated gate field effect transistors and witnessed for instance by Chapman et al (col. 4, l. 24-26). Anyone of ordinary skills in the art would consider the domain of advantage of low resistance to apply also to select gates: the operation of any gate takes less energy and time when operation is carried out under lower resistance.

In conclusion, none of applicant's arguments of traverse of the rejection of claim 1 are persuasive.

Applicant does not explain in detail any traverse of the rejection of claim 2. Therefore, Applicant's argument is not persuasive.

Applicant does not explain why cost considerations do not provide adequate motivation in the rejection of claim 3. Therefore, his argument is not persuasive.

The limitation "surround" is not the essence of claim 4, being implied already by "plurality of stacked gates and select gates arranged alternately in a row" with "the stacked gate having a control gate positioned above a floating gate". Applicant appears again oblivious of the distinction between using certain words and meeting the claim limitation. His traverse of this rejection therefore fails to persuade.

Applicant's description of claims 5 and 6 does not appear to contain any argument of traverse. Therefore, applicant's traverse is not persuasive.

Neither does his description of claim 7. The alleged erring of examiner with regard to the rejection of claim 8 is not explained except through a reference to the determination of functional language or intended use; however, why biasing would not be a matter of use is not explained at all. Applicant's traverse of the rejections of claim 7 and 8 is therefore not persuasive.

Examiner has not given patentable weight not given to specific limitations in claim 9 because of the reasons explicitly stated in the rejection with reference to case law, yet applicant does not address the specifics thereof at all. Therefore, applicant's traverse is not persuasive.

While applicant's description of claims 10-12 does not contain any argument of traverse applicant alleges "examiner has overlooked the fact that the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode and the application of specific and/or relative voltages to specific

elements are indeed structural elements" but without any explanation as to why they would be structural elements. Therefore, said argument is wholly unpersuasive.

Apart from arguments in traverse also used for claim 1, to which examiner refers by reference to the discussion of claim 1, applicant alleges "examiner is mistaken in suggesting that this structure", i.e., "the last select gate in the row being directly above the source region", "is shown in Sakui et al", despite a clear explanation by examiner with reference to a vertical line (i.e., normal to the upper main surface of the substrate) that can be drawn (Fig. 49) to intersect both source diffusion region and select gate 27. Examiner's argument is not traversed on the specifics and therefore is not persuasive.

The only point of specific traverse examiner can find in applicant's description of claims 16-19 is, or may be at best, the allegation that the references "fail to disclose or even remotely suggest a memory cell array having these features", apparently in reference to the entire enumeration of claim limitations, for which examiner refers to the foregoing discussion, and perhaps to "memory cell array", for which it suffices to refer to the fact that Hsu et al teaches a NAND Flash Memory cell array (title, abstract and column 4, line 55- column 6, line 24, as mentioned in the previous action on the merits (page 17).

Applicant does not put forward any specific argument of traverse in his discussion of claims 20-22 and 24.

Finally, although examiner apologizes for having omitted claim 24 in the heading, a detailed rejection under 35 USC 103(a) was included in the previous office actions as

admitted and noted by applicant, and the "rejected" status was clearly indicated on Form 326.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

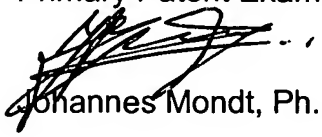
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
May 10, 2007

Primary Patent Examiner:



Johannes Mondt, Ph. D. (TC3600, AU3663)